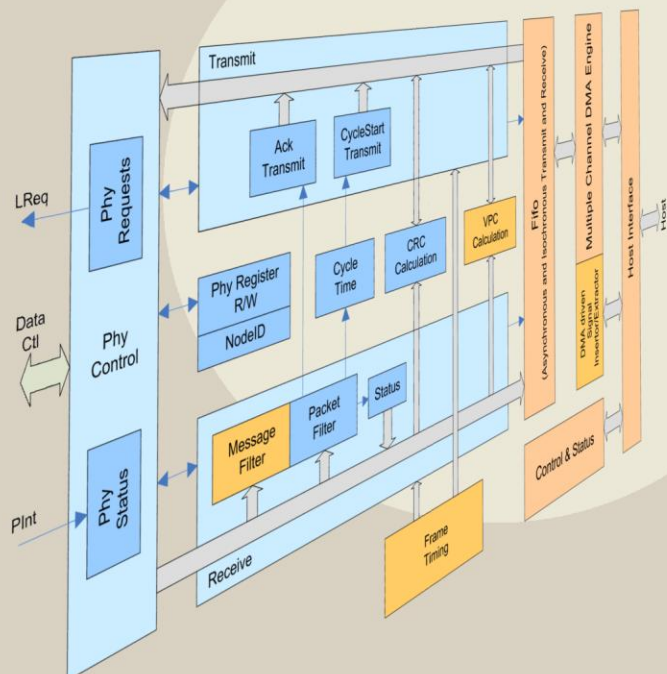




1394 IP SOLUTIONS

FIRELINK



INTRODUCTION:

This datasheet describes the FireLink® IEEE1394b Link Layer Controller Core from DapTechnology. The synthesizable IP core is based on the Link Layer Controller that has been used for several years in the FireWire analyzers produced by DapTechnology. And since its release the code has been successfully used within several 1394 applications. The code is written in VHDL and evaluation platforms are currently available for Xilinx and Altera FPGAs.

Currently, the FireLink® LLC provides the control for transmitting and receiving 1394 packets, including asynchronous packets, isochronous packets and PHY packets, at speeds up to 800 Mbps (S800). Support for S1600 and S3200 is currently in Beta stage and are expected to be released shortly.



DapTechnology introduces two versions of the Link Layer Controller to the market, i.e. a *Basic* and an *Extended* version. The Basic version is optimized for small core sizes whereas the Extended version aims for high bandwidth throughput. Both versions have their respective feature sets and benefits. DapTechnology will gladly assist customers in selecting the appropriate version for their particular product.

Key Features

- IEEE 1394-1995, 1394a-2000, 1394b-2002, 1394-2008 compliant
- Supports 100, 200, 400, 800, 1600 (beta stage) and 3200 (beta stage) Mbps data transfer rates
- Supports Legacy and Beta packets RX/TX (depending on the connected PHY)
- Software support via Dap's own 1394 SW stack FireStack®
- Supports all standard 1394 packet types
- Configurable Cycle Master capability
- Maximum isochronous packet size 8KB (S800), 16KB (S1600) and 32KB (S3200) (for Basic version & depending on buffer size)
- Isochronous and Asynchronous packet filters
- Automatic Acknowledge generation depending on Link Layer Controller state, packet type and available buffer size
- Various forced errors, including:
 - Header CRC error
 - Data CRC error
- PHY clock optional asynchronous to host clock
- Basic: Isochronous transmit/receive ports for up to 8 channels
- Compatible with Texas Instruments Physical Layer Controllers



Several market segments can leverage the DapTechnology FireLink® IP Core due to the unique features of the solution. Good examples are Aerospace & Defense, Industrial, and Consumer Electronics

industries.. As a special option, the FireLink® LLC Extended offers Firmware Support for the SAE AS5643 (Mil1394) protocol. While current implementations require significant host SW support, the FireLink® can support this layer with significantly better timing as well as reduced host resource utilization. Typical examples of applications in aerospace & defense for the FireLink® would include command & control systems for space-based vehicles, missile platforms, and fighter aircraft, as well as its implementation in avionics & IFE platforms for military, business and commercial aircraft.

COMMON FEATURES:

Host Bus Interface

Three types of host bus systems are supported

- *Generic*: A generic 32-bit synchronous host bus.
- *PLB*: A 64-bit synchronous bus used in Xilinx FPGAs for their MicroBlaze and PowerPC processors.
- *Avalon*: A 32-bit synchronous bus used in Altera FPGAs for their NIOS processor.

The Basic version is implemented as a slave-only bus interface, while the Extended version, however, utilizes a DMA engine which accesses the bus as a Master.

Control Status

Both versions have a number of registers that can be written or read. These registers are used to control the Link Layer Controller and to check its status. For the Extended version, control for the DMA engine is also provided.

CRC Calculation/Verification

Data and Header CRC are automatically added for Outgoing Packets. CRCs are verified for incoming packets. Faulty packets are ignored. Additionally errors can be injected for TX packets (header and or data CRC).

Ack Generation

Acknowledge Packet Generation is based on incoming packet content, available buffer space as well as LLC state.

Filtering

NodeID (async) and channel number (iso) specific packet filter engine.

ISO Ports (Basic version only)

A total of eight (8) independent ISO Receive and/or ISO Transmit ports are provided. The purpose of these ports is to connect dedicated stream HW (e.g.: image/video generating/receiving HW) for the handling of data streams without burdening the host processor.

Received and Transmitted isochronous packets can be routed through the ISO Ports therefore providing a dedicated and highly efficient data path for the isochronous packets. Optionally the packet headers will be skipped (RX) or automatically generated (TX).

Cycle Start Generation (optional)

A Cycle Start Packet generation functionality with its associated Cycle_Time Register is supported by the HW. The feature can be enabled disabled as needed.

Other Options

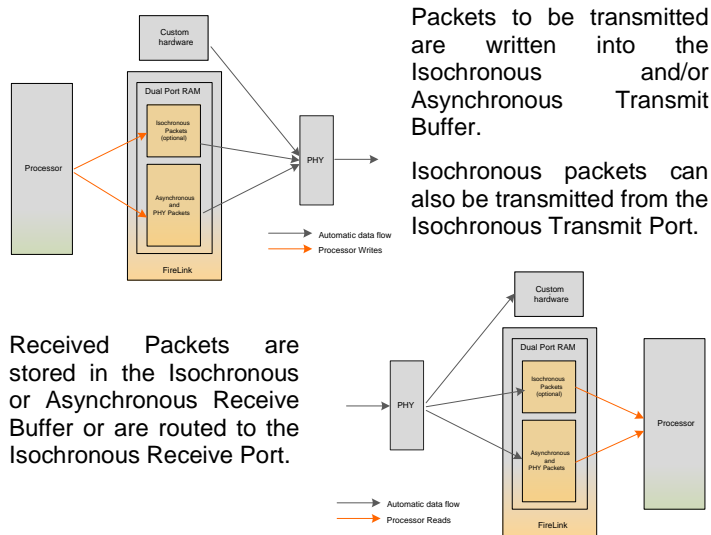
Please discuss other requirements with Dap Technology. We will provide you with a feasibility analysis as well as involved costs/lead times.

THE BASIC VERSION:

A processor driven communication:

In the *Basic* version the packet data flow is processor driven, i.e. any received/transmitted packets have to be read from or written to a Dual-Ported RAM Buffer. The Dual Port RAM Buffer is located inside the core and is customizable in size to accommodate for the maximum packet size.

This concept is ideal for small core sizes.



Architecture:

FireLink[®] Basic consists of a fully IEEE1394-2008 compliant Link Layer implementation. All LLC related functional blocks (top section in the right hand graphic) ensure functional standard compliance as well as interoperability with off-the-shelf physical layer devices (assuming PHY layer I/O compliance).

Essential to FireLink[®] Basic is its very simple host connectivity. Via a simple 32 bit data/address bus R/W operations as well as control register updates can be handled via a dual-ported RAM or direct register access. Since any communication with this DPRAM is host processor driven this interface is optimized for small/medium sized data (isochronous, asynchronous and PHY layer) packets as well as low bandwidth requirements. Just like sending large amounts of data via the I/O bus, an increased number of individual bus transactions negatively affect the overall interface performance. For transmission and reception of large isochronous streams (e.g. video and/or audio) alternate data paths are available via the ISO Transmit and Receive Ports. They allow connecting dedicated data generating/processing HW directly to the transmit/receive engines of FireLink[®]. As these dedicated ports are bypassing the host main processor they are not restricted by performance limitations of the main host interface and therefore guarantee optimized data rates.

An additional benefit is the ability to customize several functional elements of the core. Since not all 1394 implementations require a full featured 1394 interface (e.g. a pure IPv4 (IP over 1394) or Mil1394 implementation using only asynchronous messaging can reduce FPGA footprint requirements by leaving out certain functional blocks like isochronous data ports, Cycle Timer and transmit, etc. in the deployed netlist. Likewise, an isochronous data transmitting video camera can omit a RX iso port as it is a dedicated data streaming device and the general purpose RX and TX buffer can be held small.

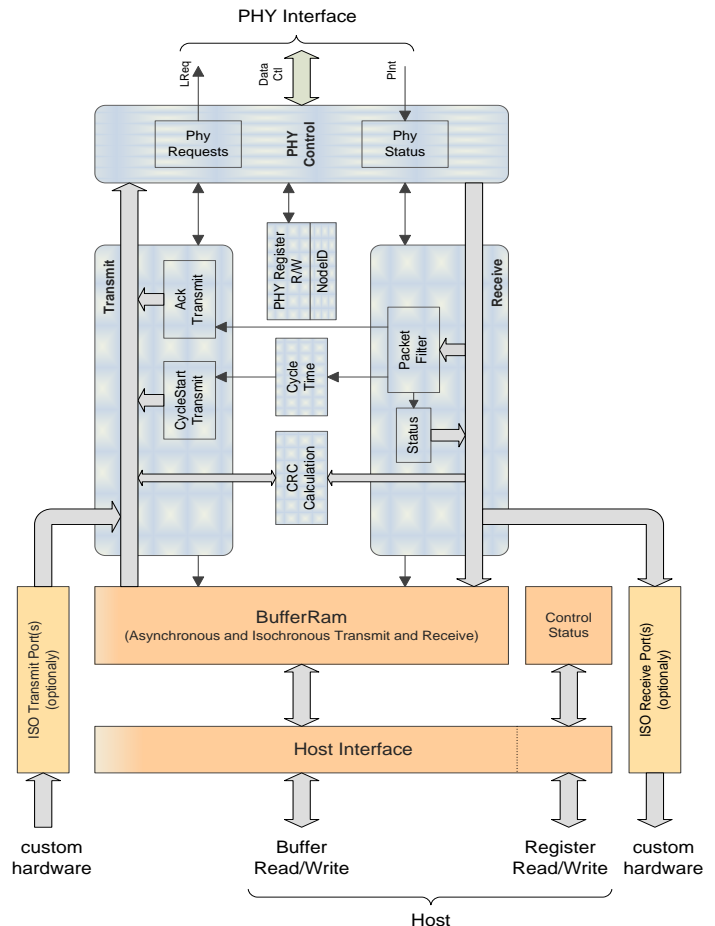
Technical Specification

	Basic Version
LUTs ²	1400 – 2000
FFs ²	700 - 1300
Block RAMs ^{2,3}	1 - 128
Host Bandwidth ¹	100 MByte/s (peak)
Buffer/FIFO size ²	1K - 64K
# of DMA channels	-
Supported FPGA platforms	Xilinx: Spartan2, Spartan3, Spartan 6, Virtex-E, Virtex-2, Virtex-4, Virtex-5, Virtex-6 Altera: Cyclone, Cyclone II/III, Stratix, Stratix II

¹ depends on host bus interface

² depends on FPGA type and selected options

³ depends on needed FIFO size

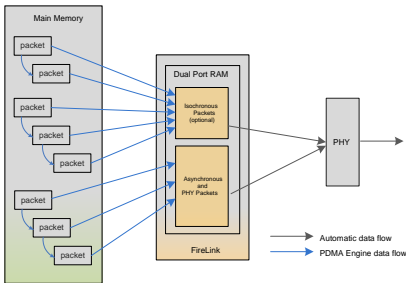


THE EXTENDED VERSION:

A DMA driven communication

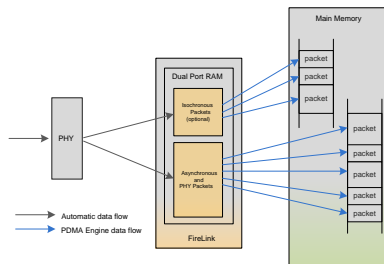
In the *Extended* version the packet data flow is DMA driven. It is a OHCI subset implementation this using descriptors and packet buffers, The LLC's DMA Engine handles the transfer to/from a FIFO Buffer for receiving and sending packets automatically, enabling high bandwidth systems. The user creates lists of packets to be sent and/or cyclic buffers for packets to be received. The FIFO is located inside the core and its size is customizable to accommodate host bus latency.

This concept is ideal for high traffic bandwidth.



Received packets are stored in chained buffers which are prepared in host memory.

A new buffer can be used for each packet, or multiple packets can be stored in one buffer.



Technical Specification

	Extended Version*
LUTs ²	2200 - 3000
FFs ²	1500 - 1900
Block RAMs ^{2,3}	1 - 128
Host Bandwidth ¹	400 MByte/s (peak)
Buffer/FIFO size ²	1K - 64K
# of DMA channels	4 - 68
Supported FPGA platforms	Xilinx: Spartan2, Spartan3, Spartan 6, Virtex-E, Virtex-2, Virtex-4, Virtex-5, Virtex-6 Altera: Cyclone, Cyclone II/III, Stratix, Stratix II

¹ depends on host bus interface

² depends on FPGA type and selected options

³ depends on needed FIFO size

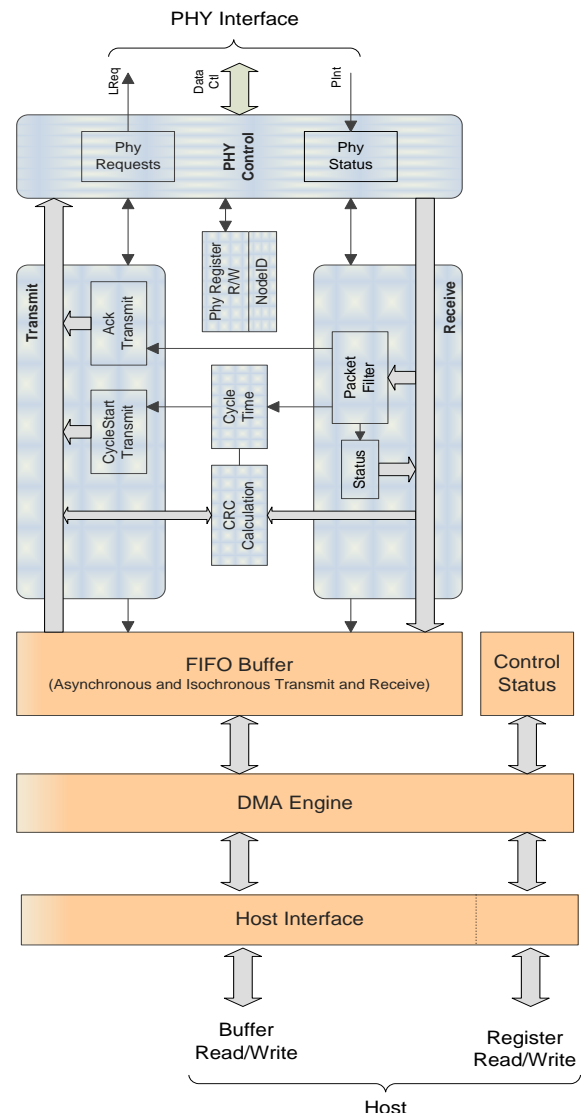
* details to be finalized

Architecture:

FireLink[®] Extended and Basic both contain the same LLC related functional blocks (top section in the right hand graphic) and with that ensure functional standard compliance as well as interoperability with off-the-shelf physical layer devices (assuming PHY layer I/O compliance).

The big difference between the two versions lies in the host connectivity interface. FireLink[®] Extended utilizes the architectural and performance-based benefits of the DMA capable communication interface. DMA transfers copy blocks of memory from one device to another and, while the CPU initiates the transfer by issuing a DMA command, it does not execute it. Advanced bus designs such as PCI typically use bus mastering DMA where the device takes control of the bus and performs the transfer itself. In an embedded processor or multiprocessor system-on-chip, it is a DMA engine connected to the on-chip bus that actually administers the transfer of the data. Another difference is that the Extended version does not include iso ports as the DMA mechanism efficiently handles the iso data transfer.

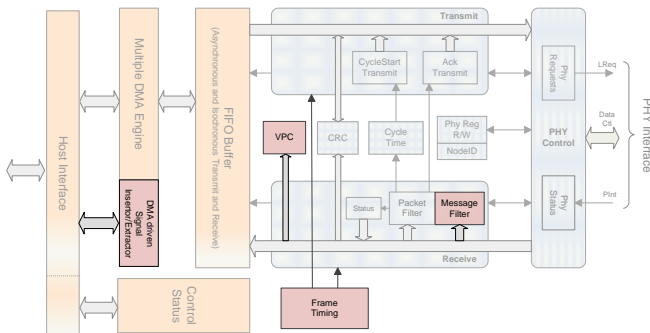
FireLink[®] Extended uses such an advanced DMA-enabled interface. And FireStack[®] - Dap's own IEEE1394 software stack – takes this concept even further with its consistent utilization of zero-copy data handling mechanisms. Together they form a very powerful combination aimed at complete system throughput optimization as well as minimization of system latencies and resource utilization.



MIL1394 EXTENSION:

As the only vendor worldwide, DapTechnology offers a very unique, but extremely powerful addition to its standard 1394b link layer IP core (extended version only). Our active participation in SAE ASD AS-1A3 standards committee together with the close collaboration with many adopters of the said standard allows DapTechnology to, not only develop a fully standards- compliant extension to the LLC, but also go beyond and/or deviate from the current AS5643 standard.

Mil1394



Mil1394 additions to extended version of FireLink LLC

The Mil1394 package is designed to offload the AS5643 support for the host processor. The following features are supported in firmware:

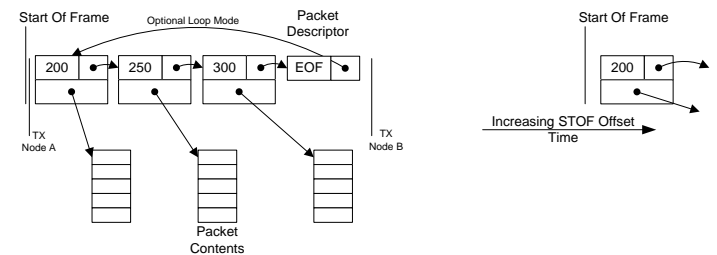
- AS5643 Protocol timing
 - STOF Generation: Accuracy: 0.3 μ sec
 - TX Frame Offset Time: 0.3 μ sec
 - RX Frame Offset Time Stamps: Accuracy : 0.3 μ sec
- AS5643 Protocol encapsulation
 - Vertical Parity Check Insertion and Verification
 - Automated STOF/ASM Field Insertion/Extraction (Heartbeat, Vehicle Time, Status Fields) - pending
 - Automated Field Value Updates (Heartbeat, Vehicle Time) - pending
- Hardware RX Filter on MessageID and/or Channel

Compared with other implementations using off-the-shelf 1394 LLC silicon (and AS5643 support implemented in SW) this Mil1394 extension to the extended version of FireLink drastically improves the overall system performance, offloads host processor and guarantees timing latencies that otherwise can only be accomplished with real-time operating systems.

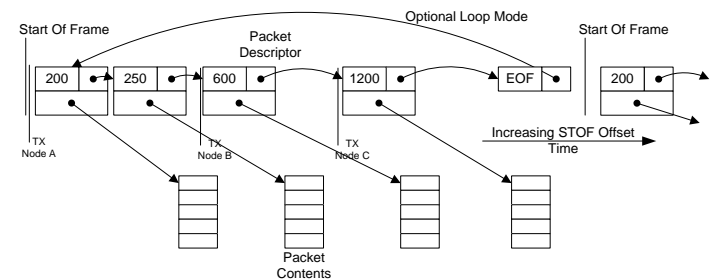
FireLink can also be paired with FireGate. With their respective Mil1394 extensions they form the perfect PHY/LLC system on the chip (SOC) solution for typical aerospace applications. Please contact DapTechnology if your requirements go beyond the current AS5643 specification. The flexible architecture of the Mil1394 extensions allows for the integration and support of features/functions that were not considered in the AS5643 standard as they are not supported by standard silicon. Examples could be static LinkIDs (instead the very dynamic nodeIDs), isochronous stream acknowledgements, Bus Reset suppression and static nodeID assignments (only suitable fully deterministic systems) as well as full System Integrity Management.

MIL1394 MESSAGING:

The Mil1394 solution takes full advantage of the OHCI-like system architecture of the extended version of the FireLink[®]. From an applications point of view the OHCI-like descriptor block model is perfectly suited for powerful transmission link lists for isochronous stream packets. Part of the descriptor is a 16 bit timing field which allows for a precise time adjustment for AS5643 transmit offset requirements. Additionally, the descriptor can be run in a looped mode in case a device has to transmit in every STOF frame.

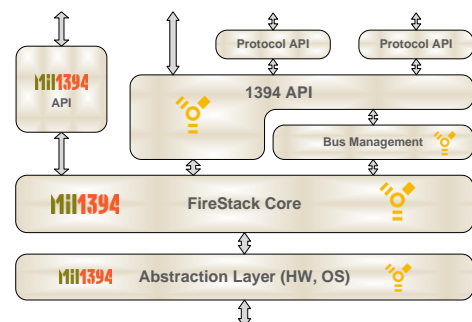


The same mechanism also allows transmitting messages from a single device but utilizing different node specific time slots. Such transmission lists can be perfectly used for simulation projects that may want to simulate an entire network's traffic without physically using multiple bus devices.



SOFTWARE SUPPORT:

In order to support Fire Link DapTechnology has developed its own SW solution FireStack[®]. This innovative SW stack was architected from ground up in order to support the advanced features of the FireLink[®] IP (Basic and Extended) solution. It complies with IEEE1394 requirements as well as select higher protocol layers e.g. IIDC). And as the only product in the market it natively supports Mil1394 (AS5643) features and functions.



PRODUCT POSITIONING:

This FireLink® IP Core is targeted for applications with up to 3200 Mbps data transmission requirements and for designs with or without PCI Link Controller requirement. Currently, there is no non-PCI compliant, general purpose silicon available for S800 or higher. FireLink® was initially designed to fill this gap. Any existing designs based on the (TSB12LV32) will greatly benefit as the FireLink® architecture shows many similarities. And with the Extended version, products requiring DMA capabilities can easily be paired with a off-the-shelf PCI IP cores or bridge chips.

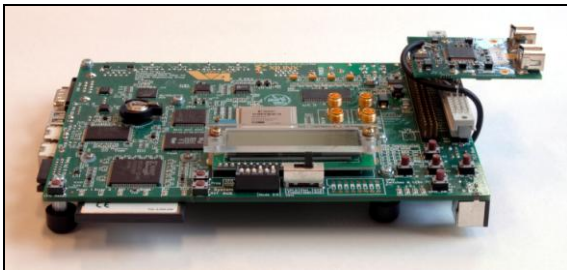
The industrial applications of FireLink® are quite broad and include robotics, machine vision, wide format digital printing and medical imaging. Finally, the FireLink® LLC Core is ideal for use in Consumer Electronics equipment such as Set Top Boxes, DVD peripherals and High Definition A/V equipment.

FireLink® is the only existing IP solution to take IEEE1394 beyond S800. And with FireGate® and FireStack® it offers a complete package for a complete 1394 bus I/O solutions able to address the growing demands for speeds beyond S800.

Evaluation Platform:

A special Evaluation Platform based on the Xilinx ML403 platform is available. Powered by the V4FX12 device and supported by industry-standard peripherals, connectors and interfaces, the Virtex-4 ML403 FX Evaluation Platform provides a great entry-level environment for developing embedded designs based on the Virtex-4 FX FPGA.

The 1394b physical layer extension is accomplished via a 1394b PHY adapter board EZPHY800. A TSB81BA3 PHY from Texas Instruments is mounted on the add-on board that is delivered with the package.

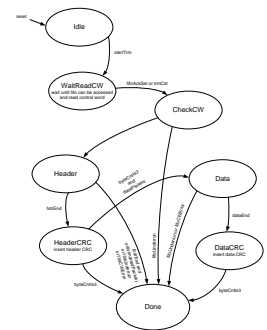


Configuration	Xilinx ML403 plus PHY Adapter board
FPGA Device	XC4VFX12-FF668-10C
1394 PHY Adapter	TSB81BA3 (or TSB41BA3)
Standard Interfaces	4 SMA Connectors (Differential Clocks), 2 PS/2 Connectors (Keyboard/Mouse), 2 Audio (In/Out, Microphone/Head Phone), RS-232 Serial Port, 3 USB Ports (2 Peripheral/1 Host), PC4 JTAG, DB 15 VGA Display, 10/100/1000 RJ-45 Ethernet Port, 64 Bit User Expansion Connector,
Package Content	ML403, 1394 PHY adapter (EZPHY)
	Universal AC/DC Adapter
	1394 Cable
PartNumber	LLC800-Eval

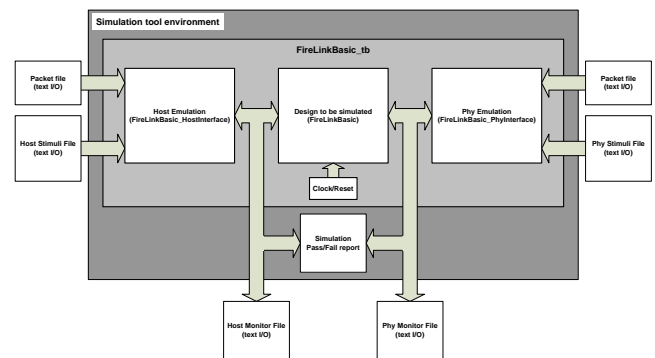
Check directly with DapTechnology for availability of Altera platforms.

VERIFICATION & TESTBENCH:

DapTechnology's FireLink® IP core includes a state-of-the-art verification and simulation suite. The entire product has been developed using stringent test criteria and procedures which are applied in all different stages, i.e. design, simulation and actual implementation.



A special VHDL Testbench has been developed and is made available to our customers for their own test and verification tasks. It mainly targets the host emulation, the LLC layer and the PHY Emulation. Test vectors (I/O files) can be used to stimulate these segments independently.



- Automated transaction based system simulation
- Easy to use pass/fail reporting
- Detailed analysis possibility presenting waveforms and signals
- RTL level functional/behavioral simulation
- Post synthesis, Netlist level functional/behavioral simulation
- Post place and route, Netlist level timing simulation possibility
- Test bench implementation done by people not involved in the implementation of the actual design

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